What is claimed is:

1. A method for forming multiple oxide layers, comprising the steps of:

forming a first gate oxide layer with a first predetermined thickness on a semiconductor substrate;

forming a first masking layer on the first gate oxide layer, the first masking layer defining a first region of the first gate oxide layer;

performing nitridation to a surface of a second region of the first gate oxide layer exposed by the first masking layer;

removing the first masking layer;

forming a second masking layer covering the first and the second regions of the first gate oxide layer but exposing a partial portion of the second region, the partial portion being defined as a third region of the first gate oxide layer;

exposing a surface of the semiconductor substrate by etching the third region of the first gate oxide layer exposed by the second masking layer; and

forming a second gate oxide layer with a second predetermined thickness on the exposed semiconductor substrate and the first region of the first gate oxide layer to thereby form a third gate oxide layer on the first region with a thickness combined of the first predetermined thickness and the second predetermined thickness.

2. The method as recited in claim 1, wherein the step of performing the nitridation to the surface of the second region of the first gate oxide layer uses a plasma nitridation technique.

3. The method as recited in claim 2, wherein the plasma nitridation technique uses a source gas containing nitrogen selected from a group consisting of N_2, NO, N_2O, NH_3, NF_3 or a mixed gas of the above or a mixed source gas obtained by adding O_2 or O_3 to the source gas.

4. The method as recited in claim 2, the plasma nitridation technique includes nitrogen flowed in a range between about 5 sccm to about 500 sccm.

5. The method as recited in claim 2, wherein the plasma nitridation technique generates plasma by supplying a source power ranging from about 100 W to about 1000 W and a bias power ranging from about 0 W to about 10 W, and is carried out with a semiconductor substrate temperature ranging from about 0 °C to about 600 °C for about 5 to about 500 seconds.

6. The method as recited in claim 1, wherein the step of exposing the surface of the semiconductor substrate by etching the third region is carried out by using a wet dip-out technique.

7. The method as recited in claim 6, wherein the wet dip-out technique uses wet chemicals such as HF based family or BOE based family.